

claim 21 in the Content of Specification portion of the Office Action. Both the original and corrected claims sections comprise specification pages 14-18.

The Examiner rejects claims 1-24 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-39 of U.S. Patent Application 09/788,211.

A timely filed terminal disclaimer can be used to overcome a rejection based on a double patenting ground provided that the conflicting patent is shown to be commonly owned with the application. The subject application is owned by Analog Devices, Inc., such assignment being recorded at Reel 011830, Frame 0665. U.S. Patent Application No. 09/788,211 is also owned by Analog Devices, Inc., such assignment being recorded at Reel 011827, Frame 0668. Accordingly, the subject application and U.S. Patent Application No. 09/788,211 are commonly owned by Analog Devices, Inc.

Enclosed herewith is a Terminal Disclaimer to obviate a provisional obviousness-type double patenting rejection over a co-pending patent application. Applicant submits that the Terminal Disclaimer overcomes the Examiner's rejections.

The Examiner rejects claims 1-24 under 35 U.S.C. §103 (a) as being obvious over *Emmerich* (U.S. Patent No. 5,392,218) in view of *Minegishi* (U.S. Patent No. 5,966,297) and in further view of *Scott* (U.S. Patent No. 5,870,046).

The Applicant's claim 1 recites an "isolation system" comprising an "isolation barrier circuit", a digital input signal ("input for receiving a digital signal") (claim 1, line 5) and a "digital output signal" (claim 1, line 8). Claim 1 also recites that the isolation system comprises a "digital to analog circuit...for receiving an input digital signal to be communicated across the isolation barrier [circuit]" (claim 1, lines 4-6) and comprises an

“analog to digital circuit having an input coupled to the analog output of the isolation barrier [circuit] for providing a digital output signal” (claim 1, lines 7-8). The digital input signal is converted to an analog signal that is communicated across the isolation barrier circuit and reconverted back to the digital output signal.

The *Emmerich*, *Scott* or *Minegishi* references, separately or combined, fail to teach or suggest an isolation barrier system comprising a digital input and a digital output signal. Nor do these references teach or suggest the conversion of a digital signal to an analog signal for communication over an isolation barrier circuit as recited in Applicant’s claim 1.

Furthermore, Applicant’s claim 12 recites “a common mode interference sensing circuit and a summing circuit” for removing the common mode interference signal from the received analog signal from the isolation barrier”. None of the references teach or suggest any sort of a common mode interference sensing circuit or summing circuit for removal of common mode interference from signals being processed.

Emmerich, for example, does not teach or suggest processing a digital input signal as claimed by the Applicant. Instead, *Emmerich* describes a “data acquisition system which provides an analog isolation barrier capable of sensing slow moving analog (essentially [DC] signals” (underline added) (column 2, lines 31-34). The “input signal is a DC value (at least with respect to the 1 mS cycle time) and the reference is scanned from the lowest possible input voltage to the highest. This takes place during the first half cycle of the basis waveform” (column 9, lines 47-51). Furthermore, *Emmerich* makes no reference to a common mode interference signal sensing circuit nor a summing circuit for removing the common mode interference signal from the signal being

communicated across its isolation barrier.

Scott does not teach or suggest processing a digital input signal nor a digital output signal as claimed by the Applicant. Instead, *Scott* processes both an analog input and an analog output signal. *Scott* describes an isolation system comprising an “input connected to an analog signal containing information to be communicated across the isolation barrier” (column 24, lines 15-16) and “resulting in an analog output 218 of the capacitive isolation system” (column 12, lines 60-61). Furthermore, *Scott* makes no reference to a common mode interference signal sensing circuit nor a summing circuit for removing the common mode interference signal from the signal being communicated across its isolation barrier.

Minegishi does not teach or suggest processing a digital input signal or a digital output signal as claimed by the Applicant. Instead, *Minegishi* describes the processing of both an analog input and an analog output signal. *Minegishi* states “the floating analog input signal is reproduced as the nonfloating reproduced analog output signal” (column 3, lines 24-26). Furthermore, *Minegishi* makes no reference to a common mode interference signal sensing circuit nor a summing circuit for removing the common mode interference signal from the signal being communicated across its isolation barrier.

The Applicant’s independent claim 21 recites an “a bi-directional isolation system” comprising a “first” and a “second digital to analog circuit” and a “first” and a “second analog to digital circuit”. Applicant’s claim 22 depending from claim 21 recites signals that “are communicated simultaneously across the isolation barrier circuit”. Applicant’s claim 24 depending from claim 21 recites an “echo cancellation circuit for removing a local echo signal from the input of at least one of said first and second analog

to digital circuits”.

The *Emmerich*, *Scott* or *Minegishi* references, separately or combined, fail to teach or suggest a bi-directional isolation system comprising first and a second digital to analog circuit and a first and a second analog to digital circuit. Neither *Emmerich* nor *Minegishi* describe a bi-directional isolation system. *Scott* only describes a bi-directional system that is multiplexed, and does not provide simultaneous communication in both directions as provided for by the Applicant’s claimed invention. None of the references teach or suggest any sort of echo cancellation circuit.

Regarding claims 2-20 and 22-24, these claims distinguish over the prior art because, at minimum, they are dependent from claims 1 and 21 respectively, which are respectfully asserted to distinguish over the prior art as explained above. Furthermore, many if not all of the elements of claims 2-20 and 22-24 distinguish over the combination of *Emmerich*, *Scott* or *Minegishi* independently of their association with claims 1 and 21 respectively.

For example, Applicant’s claim 2 depending from claim 1, recites that the digital to analog circuit of claim 1 includes an “encoder circuit responsive to said input digital signal to provide a digital signal”. Applicant’s claim 17, depending from claim 2, recites that the signal of the parent claim is an “constant average signal”.

Applicant’s claims 3-5 recite the use of a “modulation circuit”, “decoder” and “demodulation circuit” respectively. Likewise, the subject matter of these claims also provide and/or process a “constant average signal” as recited by their respective dependent claims 18-20. As stated in the Applicant’s specification “It was further realized that performance could be enhanced by shaping the analog signal to be transmitted through

the isolation barrier so that it exhibited a constant signal average" (page 4, lines-6-8).

The *Emmerich*, *Scott* or *Minegishi* references, separately or combined, fail to teach or suggest the subject matter recited in the Applicant's claims 2-5 and 17-20, and none of these references teach or suggest any use of a constant average signal as claimed by the Applicant.

In summary, as explained above, neither the *Emmerich*, *Scott* or *Minegishi* references, separately or combined, teach or suggest the claimed elements of the Applicant's claims 1-24.

CONCLUSION

Accordingly, independent claims 1 and 21 and dependent claims 2-20 and claims 22-24 are allowable over the cited art. Early and favorable action is respectfully requested. If for any reason this Response is found to be incomplete, or if at any time it appears that a telephone conference with counsel would help advance prosecution, please telephone the undersigned or his associates, collect in Waltham, Massachusetts, at (781) 890-5678.

Respectfully submitted,



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